ADVANCE

CY8CTST242

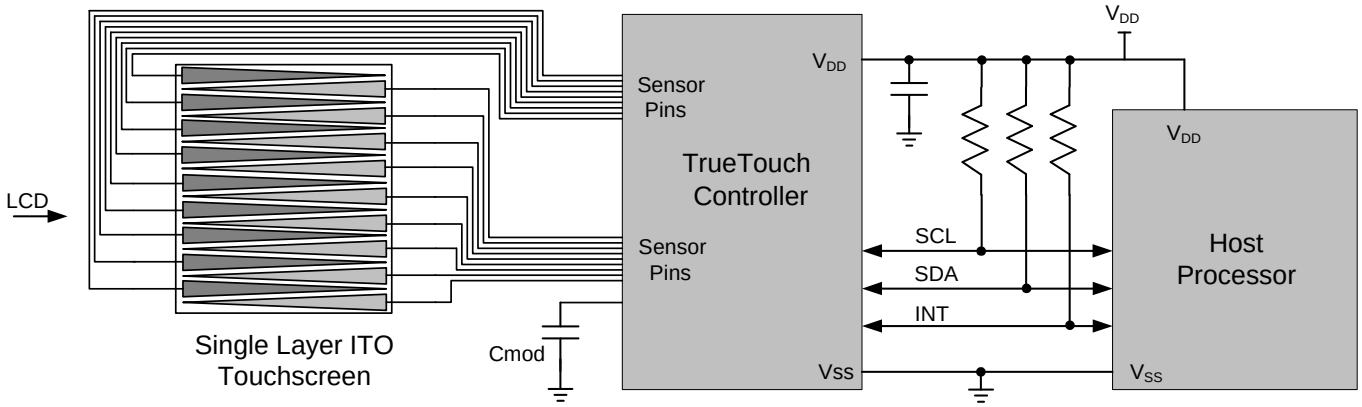
TrueTouch™ Single Touch Touchscreen Controller

Features

- TrueTouch™ capacitive touchscreen controller
  - True single layer ITO sensor support - no bridges
    - Lowers touchscreen system cost
  - Single finger position reported
    - X, Y positions and Z magnitude reported
  - Screen sizes up to 3.5" diagonal
  - Up to 32 sense pins
  - Fat finger detection and tracking
  - Large object detection
  - Self-calibrating to environmental changes
  - Resistant to LCD noise
  - Robust operation in noisy RF environment
  - 1.71 V to 5.5 V input supply range
    - Single supply voltage
    - Compatible with 1.8 V I2C signaling
    - Integrated voltage regulators – no need for dedicated voltage regulators
- Performance
  - Noise-free resolution: 0.2 mm
  - Accuracy with 1 finger on the touchscreen: 1.25mm
  - >110 Hz refresh rate with 1 finger on the touchscreen
  - Best in class active power of 3.6 mW
  - Best in class low-power state current: 0.7 mA
  - Best in class deep sleep state current: 100 nA
- Extended feature set
  - Water rejection - no false touches
  - Capacitive buttons supported
  - On-chip gesture detection
    - Single-click, double-click
    - One-finger pan gestures
    - 2 finger Pinch/Zoom gestures

      Second finger co-ordinate reported to support operating system gesture decoding
- Sensor and system design
  - Supports chip-on-flex and chip-on-board
  - Supports plastic film and glass touch sensors
  - Supports a variety of touchscreen sensor stackups
- Communication interface
  - I2C slave up to 400 kHz
  - SPI slave with 2 Mbps sustained data throughput
  - Field upgrades through integrated bootloader
- Host development kit (HDK)
  - Android driver support
  - Supports custom driver development
  - TrueTouch host emulator – acts as host for early prototyping
- Package options
  - 32-pin 5 × 5 × 0.55 mm QFN
  - 48-pin 7 × 7 × 1.0 mm QFN
  - 30-ball 2.2 x 2.32 x 0.4 mm WLCSP

CY8CTST242 Block Diagram



Contents

TrueTouch CY8CTST242 Overview **3**
Capacitive Sensing with TST242 ..... **3**
Introduction to Capacitive Touchscreens **3**
TrueTouch Features **4**
True Single Layer Sensors 4
Large Object Detection 4
Fat Finger Tracking 4
On-Chip Gesture Decoding 4
Water Rejection 4
Capacitive Buttons 4
Power States Summary **5**
Pin Information **6**
Communications Protocol Summary **9**
Operating Mode Register Map 10
System Information Mode Register Map 11
Test Mode Register Map 12
Host Development Kit (HDK) **13**
Mobile Device Operating System Driver Support **13**
Example Application Schematic **14**
Component Recommendations 14
Gestures **15**
Touchscreen System Specifications **16**
Performance Conditions 17
Electrical Specifications **18**
Absolute Maximum Ratings 18
Device Operating Temperature 18
DC Chip Level Specifications 18
DC General Purpose I/O Specifications 19
DC Analog Mux Bus Specifications 21
DC Programming Specifications 21
AC Chip Level Specifications 22
AC GPIO Output Specifications 22
AC Programming Specifications 23
I2C Specifications 24
SPI Specifications 25
Packaging Information **27**
Thermal Impedances 29
Solder Reflow Peak Temperature 29
Ordering Information **30**
Ordering Code Definitions 30
Acronyms **31**
Document Conventions **31**
Port Nomenclature 31
Bit Field Nomenclature 31
Reference Documents **32**
Glossary **33**
Document History Page **35**
Sales, Solutions, and Legal Information **35**
Worldwide Sales and Design Support 35
Products 35
PSoC® Solutions 35

TrueTouch CY8CTST242 Overview

The TrueTouch CY8CTST242 is a capacitive touchscreen controller with the sensing technology to resolve one finger on the touchscreen, report its position (X, Y, and magnitude Z) and gesture information. It converts an array of interdigitated sensors into digital values. This array of digital information is processed by touch detection and position resolution algorithms in the touchscreen controller to determine the location of the finger on the touchscreen. The position and movement of the finger is further processed and recognized as gestures such as click, double click, and pan and provided to the host. The CY8CTST242 supports two finger pinch/zoom gestures both on-chip and by reporting the finger position of a second finger. Additionally, the CY8CTST242 family supports advanced features like large finger or thumb detection, palm or face detection, and water rejection.

The touchscreen subsystem of any end product has many critical components such as the touch controller, application firmware, ITO sensor and LCD, a verified sensor design, and manufacturing test. Because of this complexity, Cypress brings significant value to each CY8CTST242 customer by providing full firmware (communications, sensing, and gesture code), and design guidance for the sensor.

The CY8CTST242 touchscreen controller interfaces with a host through an I^2C slave interface at 400 kHz or an SPI slave interface with a sustained data throughput up to 2 Mbps. The controller is optimized for low power and fast response time. Built-in support for manufacturing test is provided to ensure complete and efficient testing. Field upgrades are supported with an integrated bootloader that uses the host communications interface.

Capacitive Sensing with TST242

The CY8CTST242 is available in 30-ball WLCSP, 32-pin QFN and 48-pin QFN packages. The 30-ball WLCSP and 32-pin QFN provides up to 24 sense pins, while the 48-pin QFN provides up to 32 sense pins. The CY8CTST242 allows any ITO sense pin to be assigned to any X or Y sensor for easy circuit layout and routing.

The CY8CTST242 uses self-capacitance sensing technology, which is the capacitance from a sensor electrode to circuit ground. With the self-capacitance method, a finger placed on the sensor increases capacitance measured on the sensor. This capacitance is converted into a digital value and processed by algorithms to report finger positions and gestures.

If the algorithms detect a finger, on-chip position resolution algorithms interpolate finger position between sensors. The touchscreen resolution is firmware programmable and is typically set to match the number of LCD pixels. For example, if the display is a QVGA with 320 × 240 pixels, the touchscreen controller is also set to 320 × 240 pixels.

Introduction to Capacitive Touchscreens

A capacitive touchscreen detects changes in measured capacitance to determine the location of one or more fingers on the surface of the touchscreen. The capacitive touchscreen consists of a capacitive touchscreen sensor, a touchscreen controller, and a flexible printed circuit (FPC) that connects them together. The touchscreen sensor is positioned between the LCD and a protective cover lens that the user touches. The touchscreen sensor is normally connected to the Cypress TrueTouch touchscreen controller through an FPC that is bonded to the sensor using a conductive adhesive. The FPC is connected to the main application host processor through a connector on the host printed circuit board (PCB). The Cypress TrueTouch controller can either be affixed to this FPC, or directly on the host PCB. Users can interact with the user interface displayed on the LCD through finger movements and gestures on the surface of the protective cover lens.

A capacitive touchscreen sensor commonly uses a multilayer plastic film/glass construction or a single-layer glass construction. The capacitive sensor is typically created with a transparent conductive material called indium tin oxide (ITO). ITO sensors are formed on the plastic film or glass substrates in a grid of rows and columns. A thin isolation layer separates the row sensors from the column sensors. The ITO sensors are typically several hundred angstroms thick and must be handled with care to prevent damage. Experienced sensor suppliers can control the deposition to achieve thin, transparent sensors, while optimizing sensing performance. Metal traces run along the border of the sensor grid to connect the conductive ITO sensors to the FPC and touchscreen controller. Because the metal traces are not transparent, the cover lens requires an opaque border outlining the active area of the touchscreen.

These metal traces carry the capacitive signals to the Cypress TrueTouch controller for sensing and calculation. Some important considerations when choosing a touchscreen controller device include: 1) capacitance-to-digital conversion accuracy 2) noise handling ability and 3) processing algorithms. These controller features allow the engineer to develop a system that accurately detects finger presence, motion, and a user's intended activity on the touchscreen. Each of these features also contribute to the overall perceived performance of a touchscreen: the more precise the handling of capacitive inputs, including resisting noise when processing data into finger positions and gestures, the better the user experience.

Cypress's TrueTouch controller architecture was specifically designed to optimize capacitance-to-digital conversion accuracy, resist system noise, and provide the world's highest performance touchscreen controller. This data sheet describes the CY8CTST242 technical details that enable an engineer to create a world-class touchscreen product.

TrueTouch Features

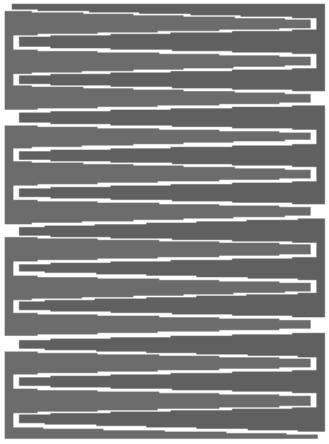
A state-of-the-art touchscreen system with a flawless user interface experience involves much more than just being able to detect a finger touch reliably. The CY8CTST242 provides several important features that allow development of highly desirable and differentiated products with exceptional touch-screen systems.

True Single Layer Sensors

Existing sensors designs either require two layers of ITO material or one layer of ITO material with bridges made of either metal or ITO. For extremely low cost designs, it is desirable to have a sensor made up of a single layer of ITO with no bridges. One possible solution is to use interlocking triangle or "backgammon" patterns as shown in Figure 1. CY8CTST242 supports bridgeless single layer sensors with single finger tracking and gestures.

Bridgeless single layer is an ITO pattern where all sensors are located in a single layer without sensors overlapping and connected by bridges. Reducing number of patterned ITO layers and bridges reduces overall system cost. The single layer sensor may or may not have a shield layer depending on LCD type and air gap.

Figure 1. Single Layer ITO Sensor Pattern with no Bridges



Large Object Detection

In many applications it is desirable to know when a large object is present on the touchscreen. Two common examples of this are touching the palm on the screen when typing, and pressing the side of the face on the screen when talking on a phone. A large object, such as a fist, palm, or side of a face, can be determined by the CY8CTST242 from the touchscreen data and an indication is sent to the host.

Fat Finger Tracking

In a well-designed touchscreen system it is important for a fat finger or thumb to be correctly detected and tracked. If this crucial feature is not supported, a fat finger can incorrectly be reported as two or more touches and hamper the user interface experience. When an object such as a thumb is pressed against the panel, the CY8CTST242 ensures that only one touch is reported in the center of the thumb.

On-Chip Gesture Decoding

The human interface to electronic devices is a rapidly evolving arena. Gone are the days of rubber buttons and unwieldy dials. The latest data entry systems use touch sensing with gesture recognition. These interfaces provide intuitive responses to touch motion over the sensing panel. The CY8CTST242 is able to decode gestures on-chip and report to the host. Gestures are determined by processing the finger position and motion data by the touchscreen controller and reported to the host as a Gesture ID. The CY8CTST242 provides a configurable library of one finger gestures:

- Single-click, double-click
- One-finger pan gestures
- Zoom in and zoom out

Water Rejection

Water droplets can cause false touches to be reported in a projected capacitive touchscreen. However, the CY8CTST242's performance does not degrade with water present on the touchscreen. No false detections will occur when water droplets are on the surface of the touchscreen. Droplet sizes ranging from 0.1 mm to 3 mm are rejected. No false touches are detected when the screen is covered with a film of water, ranging from 0.1 mm to 1 mm thickness. Condensation does not produce any false touches.

Capacitive Buttons

In many capacitive touchscreen applications it is desirable to implement capacitive touch buttons with the same touchscreen controller to save on cost. A capacitive button is a button of capacitive material separate from the touchscreen that is scanned and its presence provided to the host. Some touch-screen mobile phones implement buttons such as the ‘Home’ button as capacitive buttons. The CY8CTST242 provides the ability to add capacitive buttons that are easy to implement.

Power States Summary

The CY8CTST242 controller includes a configurable power state machine as shown in Figure 2. There are three separate states: **Active**, during which the touchscreen is actively scanned and new touchscreen data is regularly refreshed; **Low Power**, during which the touchscreen is scanned at a much slower rate to detect the presence of a finger; and **Deep Sleep**, during which the touchscreen is not scanned and the CY8CTST242 controller is in a very low power state, the internal clocks are turned off but the state of all registers and Static Random Access Memory (SRAM) is maintained. There are three parameters to configure the power state machine: Active Refresh Interval (register ACT_INTRVL) defines the minimum time between the start of subsequent touchscreen scans in the active state; Touch Timeout (register TCH_TMOUT) defines the time to stay in the Active state after the last finger is removed from the touchscreen before transitioning to the Low Power state; and Low Power Refresh Interval (register LP_INTRVL) defines the time in the Low Power state between touchscreen scans. The power state machine is active only when the CY8CTST242 controller is communicating in the operating mode. In all other communication modes, the touchscreen is scanned continuously. See section Communications Protocol Summary on page 9 for a detailed description of operating mode, system information mode, and the test mode.

At startup in Operating mode, the CY8CTST242 controller enters the **Active** power state. In the **Active** power state, the controller periodically scans the panel, determines whether it is being touched, identifies the finger centroid locations, and processes these positions and motion into gestures.

In **Active** state, the Active Refresh Interval register specifies the scanning/processing cycle interval in milliseconds. If a touchscreen can be scanned and processed in less time than specified by the Active Refresh Interval for the remaining time the controller sleeps to reduce power consumption. If the scanning/processing time exceeds the specified actual scanning/processing cycle interval by the ACT_INTRVL register, scanning/processing cycles are executed continuously without any idle/sleep time. Increasing the Active Refresh Interval value decreases power consumption in the Active state but increases touchscreen data refresh time.

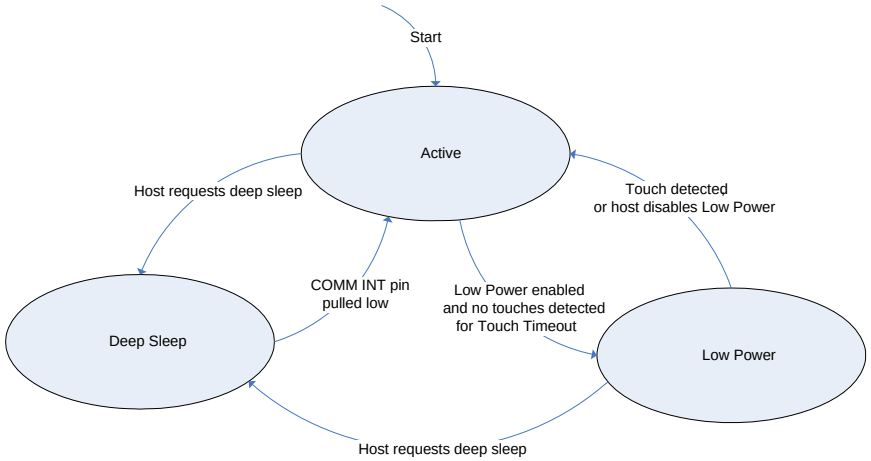
If the host sets the Low Power bit (bit 2 of the HST_MODE register) the CY8CTST242 controller automatically manages transitions from the **Active** state to the **Low Power** state, based upon finger/touch activity. The Touch Timeout specifies the minimum time duration (in 10 ms increments) the controller remains in the **Active** state after its last detection of touch activity. After no touch activity has been detected for this time duration, the controller enters the **Low Power** state.

In the **Low Power** state, the Low Power Refresh Interval defines how often the touchscreen is scanned. Unlike the Active state, in the Low Power state the finger positions are not updated after a scan, the controller is only scanning to see whether a finger is detected. When a finger is detected, the controller transitions to the active state and begins normal, regular touchscreen scanning and processing. The host may also clear the Low Power bit to force the CY8CTST242 controller out of the **Low Power** state and into the **Active** state. Also, if the host sets the Deep Sleep bit (bit 1 of the HST_MODE register) while in the **Low Power** state, the controller will transition to the **Deep Sleep** state.

To transition from the **Active** or **Low Power** states to the **Deep Sleep** state, the host must set the Deep Sleep bit, after which the CY8CTST242 controller will put itself in an ultra-low power condition instead of performing the next touchscreen scan. The controller remains in the **Deep Sleep** state until the host pulls the COMM INT pin low, after which the controller wakes up and returns to the **Active** state.

Figure 2 illustrates the three power states and their transitions. For more information on configuring the behavior of power states in the CY8CTST242, refer to the *TrueTouch™ Standard Products Platform Technical Reference Manual (TRM)*.

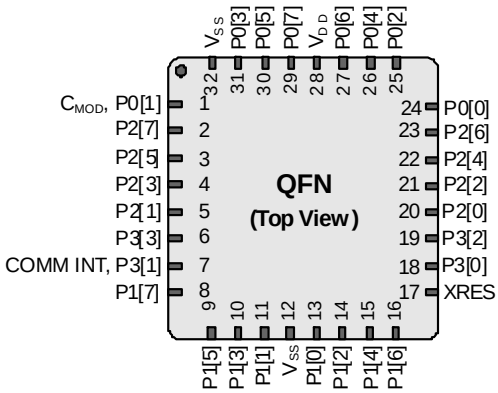
Figure 2. CY8CTST242 Power States and Transitions



Pin Information

The CY8CTST242 is available in several packages. This section provides the pin names, descriptions, and mapping to the physical package.

Table 1. 32-Pin QFN (CY8CTST242-LQI-01)

Pin No.	Name	Functions	Pin Map
1	P0[1]	C_{MOD}(Integrating input)[6]	
2	P2[7]	Sense pin multiplexable to X or Y sensor	
3	P2[5]	Sense pin multiplexable to X or Y sensor	
4	P2[3]	Sense pin multiplexable to X or Y sensor	
5	P2[1]	Sense pin multiplexable to X or Y sensor	
6	P3[3]	Sense pin multiplexable to X or Y sensor	
7	P3[1]	COMM INT (Interrupt to Host and Wake signal from Host)[5]	
8	P1[7]	I2C SCL, SPI SS, or sense pin multiplexable to X or Y sensor	
9	P1[5]	I2C SDA, SPI MISO, or sense pin multiplexable to X or Y sensor	
10	P1[3]	SPI CLK, or sense pin multiplexable to X or Y sensor	
11	P1[1]	ISSP CLK[2], I2C SCL[3], SPI MOSI, or sense pin multiplexable to X or Y sensor	
12	V_{SS}	Connect to circuit ground	
13	P1[0]	ISSP DATA[2], I2C SDA[3], SPI CLK[4], or sense pin multiplexable to X or Y sensor	
14	P1[2]	Sense pin multiplexable to X or Y sensor	
15	P1[4]	Sense pin multiplexable to X or Y sensor	
16	P1[6]	Sense pin multiplexable to X or Y sensor	
17	XRES	Active HIGH external reset with internal pulldown	
18	P3[0]	Sense pin multiplexable to X or Y sensor	
19	P3[2]	Sense pin multiplexable to X or Y sensor	
20	P2[0]	Sense pin multiplexable to X or Y sensor	
21	P2[2]	Sense pin multiplexable to X or Y sensor	
22	P2[4]	Sense pin multiplexable to X or Y sensor	
23	P2[6]	Sense pin multiplexable to X or Y sensor	
24	P0[0]	Sense pin multiplexable to X or Y sensor	
25	P0[2]	Sense pin multiplexable to X or Y sensor	
26	P0[4]	Sense pin multiplexable to X or Y sensor	
27	P0[6]	Sense pin multiplexable to X or Y sensor	
28	V_{DD}	Supply Voltage	
29	P0[7]	Sense pin multiplexable to X or Y sensor	
30	P0[5]	Sense pin multiplexable to X or Y sensor	
31	P0[3]	Sense pin multiplexable to X or Y sensor, or C_{MOD}[7]	
32	V_{SS}	Connect to circuit ground	
EP	–	Exposed pad. Connect to circuit ground, see Figure 10 on page 27 Note 1	

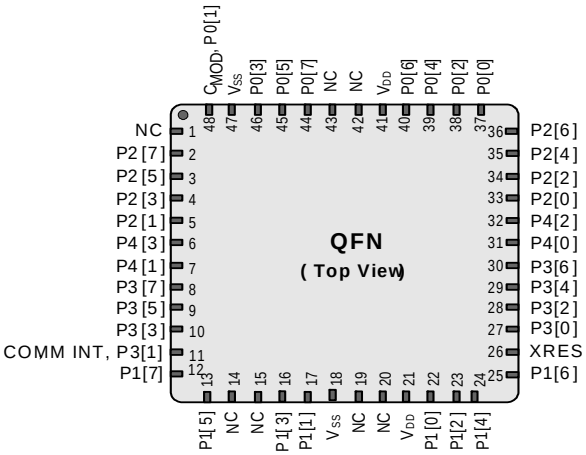
Notes

1. The center pad (EP) on the QFN package must be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
2. On power up, the ISSP SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The ISSP SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the ISSP SDA and the ISSP SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power up or reset event, P1[1] and P1[0] may disturb the I2C bus if it is on the same pins. Pins P1[7] and P1[5] are preferred for I2C to avoid this issue.
3. Alternate I2C pins, P1[7] and P1[5] are preferred to non-conforming behavior at power up described in Note 2.
4. Alternate SPI clock.
5. This pin is set to COMM INT by default, the interrupt pin can be moved to any other pin if necessary. If this pin is not used for COMM INT it may be used as a sense pin multiplexable to X or Y sensor.
6. This pin is set to C_{MOD} by default. If this pin is not used for C_{MOD} it may be used as a sense pin multiplexable to X or Y sensor.
7. This is the alternate pin for C_{MOD}.

Table 2. 48-Pin QFN (CY8CTST242-LTI-01)

Pin No.	Name	Functions
1	NC	Leave unconnected
2	P2[7]	Sense pin multiplexable to X or Y sensor
3	P2[5]	Sense pin multiplexable to X or Y sensor
4	P2[3]	Sense pin multiplexable to X or Y sensor
5	P2[1]	Sense pin multiplexable to X or Y sensor
6	P4[3]	Sense pin multiplexable to X or Y sensor
7	P4[1]	Sense pin multiplexable to X or Y sensor
8	P3[7]	Sense pin multiplexable to X or Y sensor
9	P3[5]	Sense pin multiplexable to X or Y sensor
10	P3[3]	Sense pin multiplexable to X or Y sensor
11	P3[1]	COMM INT (Interrupt to Host and Wake signal from Host)[12]
12	P1[7]	I2C SCL, SPI SS, or sense pin multiplexable to X or Y sensor
13	P1[5]	I2C SDA, SPI MISO, or sense pin multiplexable to X or Y sensor
14	NC	Leave unconnected
15	NC	Leave unconnected
16	P1[3]	SPI CLK, or sense pin multiplexable to X or Y sensor
17	P1[1]	ISSP CLK[9], I2C SCL[10], SPI MOSI, or sense pin multiplexable to X or Y sensor
18	V_{SS}	Connect to circuit ground
19	NC	Leave unconnected
20	NC	Leave unconnected
21	V_{DD}	Supply Voltage
22	P1[0]	ISSP DATA[9], I2C SDA[10], SPI CLK[11], or sense pin multiplexable to X or Y sensor
23	P1[2]	Sense pin multiplexable to X or Y sensor
24	P1[4]	Sense pin multiplexable to X or Y sensor
25	P1[6]	Sense pin multiplexable to X or Y sensor
26	XRES	Active HIGH external reset with internal pulldown
27	P3[0]	Sense pin multiplexable to X or Y sensor
28	P3[2]	Sense pin multiplexable to X or Y sensor
29	P3[4]	Sense pin multiplexable to X or Y sensor
30	P3[6]	Sense pin multiplexable to X or Y sensor
31	P4[0]	Sense pin multiplexable to X or Y sensor
32	P4[2]	Sense pin multiplexable to X or Y sensor
33	P2[0]	Sense pin multiplexable to X or Y sensor
34	P2[2]	Sense pin multiplexable to X or Y sensor
35	P2[4]	Sense pin multiplexable to X or Y sensor
36	P2[6]	Sense pin multiplexable to X or Y sensor

Pin Map



Pin No.	Name	Functions
37	P0[0]	Sense pin multiplexable to X or Y sensor
38	P0[2]	Sense pin multiplexable to X or Y sensor
39	P0[4]	Sense pin multiplexable to X or Y sensor
40	P0[6]	Sense pin multiplexable to X or Y sensor
41	V_{DD}	Supply voltage
42	NC	Leave unconnected
43	NC	Leave unconnected
44	P0[7]	Sense pin multiplexable to X or Y sensor
45	P0[5]	Sense pin multiplexable to X or Y sensor
46	P0[3]	Sense pin multiplexable to X or Y sensor, or C_{MOD}[14]
47	V_{SS}	Connect to circuit ground
48	P0[1]	C_{MOD} (Integrating input)[13]
EP	–	Exposed pad. Connect to circuit ground, see Figure 11 on page 28 Note 1

Notes

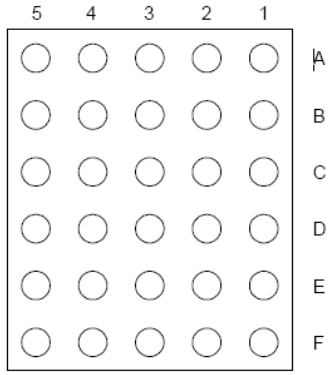
8. The center pad (EP) on the QFN package must be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
9. On power up, the ISSP SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The ISSP SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the ISSP SDA and the ISSP SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power up or reset event, P1[1] and P1[0] may disturb the I2C bus if it is on the same pins. Pins P1[7] and P1[5] are preferred for I2C to avoid this issue.
10. Alternate I2C pins, P1[7] and P1[5] are preferred to non-conforming behavior at power up described in Note 9.
11. Alternate SPI clock.
12. This pin is set to COMM INT by default, the interrupt pin can be moved to any other pin if necessary. If this pin is not used for COMM INT it may be used as a sense pin multiplexable to X or Y sensor.
13. This pin is set to C_{MOD} by default. If this pin is not used for C_{MOD} it may be used as a sense pin multiplexable to X or Y sensor.
14. This is the alternate pin for C_{MOD}.

Table 3. Pin Definitions – CP8CTST242-FNC-01 30-Ball Part Pinout (WLCSP)

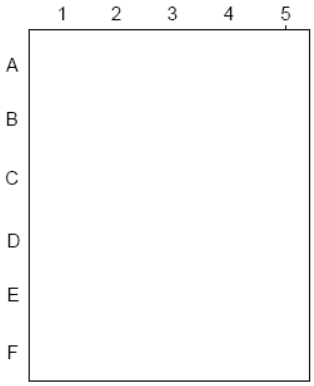
Pin No.	Name	Description
A1	P0[2]	Sense pin multiplexable to X or Y sensor
A2	P0[6]	Sense pin multiplexable to X or Y sensor
A3	V_{DD}	Supply voltage
A4	P0[1]	CMOD (Integrating input)[15]
A5	P2[7]	Sense pin multiplexable to X or Y sensor
B1	P2[6]	Sense pin multiplexable to X or Y sensor
B2	P0[0]	Sense pin multiplexable to X or Y sensor
B3	P0[4]	Sense pin multiplexable to X or Y sensor
B4	P0[3]	Sense pin multiplexable to X or Y sensor, or CMOD[16]
B5	P2[5]	Sense pin multiplexable to X or Y sensor
C1	P2[2]	Sense pin multiplexable to X or Y sensor
C2	P2[4]	Sense pin multiplexable to X or Y sensor
C3	P0[7]	Sense pin multiplexable to X or Y sensor
C4	P0[5]	Sense pin multiplexable to X or Y sensor
C5	P2[3]	Sense pin multiplexable to X or Y sensor
D1	P2[0]	Sense pin multiplexable to X or Y sensor
D2	P3[0]	Sense pin multiplexable to X or Y sensor
D3	P3[1]	COMM INT (Interrupt to Host and Wake signal from Host)[17]
D4	P3[3]	Sense pin multiplexable to X or Y sensor
D5	P2[1]	Sense pin multiplexable to X or Y sensor
E1	XRES	Active HIGH external reset with internal pulldown
E2	P1[6]	Sense pin multiplexable to X or Y sensor
E3	P1[4]	Sense pin multiplexable to X or Y sensor
E4	P1[7]	I2C SCL, SPI SS, or sense pin multiplexable to X or Y sensor
E5	P1[5]	I2C SDA, SPI MISO, or sense pin multiplexable to X or Y sensor
F1	P1[2]	Sense pin multiplexable to X or Y sensor
F2	P1[0]	ISSP DATA[18], I2C SDA[19], SPI CLK[20] or, sense pin multiplexable to X or Y sensor
F3	V_{SS}	Supply ground
F4	P1[1]	ISSP CLK[18], I2C SCL[19], SPI MOSI[20], or sense pin multiplexable to X or Y sensor.
F5	P1[3]	SPI CLK, or sense pin multiplexable to X or Y sensor.

Pin Map

Bottom View



Top View



Notes

15. This pin is set to C_{MOD} by default. If this pin is not used for C_{MOD} it may be used as a sense pin multiplexable to X or Y sensor.
16. This is the alternate pin for C_{MOD}
17. This pin is set to COMM INT by default, the interrupt pin can be moved to any other pin if necessary. If this pin is not used for COMM INT it may be used as a sense pin multiplexable to X or Y sensor.
18. On power up, the ISSP SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The ISSP SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the ISSP SDA and the ISSP SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power up or reset event, P1[1] and P1[0] may disturb the I2C bus if it is on the same pins. Pins P1[7] and P1[5] are preferred for I2C to avoid this issue.
19. Alternate I2C pins, P1[7] and P1[5] are preferred to non-conforming behavior at power up described in Note 2.
20. Alternate SPI clock.

Communications Protocol Summary

A key aspect of the CY8CTST242 touchscreen controller is the communications protocol, as defined by the register maps for each of the following three modes of communications.

- Operating mode
- System Information mode
- Test mode

The CY8CTST242 supports both I^2C and SPI with the same communications modes and register maps The communication mode controls the operation of the CY8CTST242 and the information it reports to the host. The CY8CTST242 has a large amount of information available; however, only a very small subset of that information is needed during normal operation of the device. To optimize the data communication between the touchscreen controller and the host, the information is split into multiple modes. The operation of these modes and the data they communicate is summarized below and in the register map tables that follow. For more information on CY8CTST242 protocols and the details of all registers, refer to the TrueTouch™ Standard Products Platform Technical Reference Manual (TRM).

Each communication mode has both unique data/registers and one or more registers in common with other communications modes. All modes share the Host Mode register (HST_MODE). This register is used by the host to: command the CY8CTST242 to change communications mode, enable the Low Power state, command a transition to Deep Sleep state and command a soft reset of the controller.

In **Operating** mode all of the necessary information for receiving and controlling touch coordinates and gestures is provided, in addition to control over the power states via access to the Host Mode register. The only time it would be necessary for a device to exit this device mode would be for the retrieval of system information, for instance at system start-up, or to perform some kind of system test or self-test.

The information available to the host in operating mode is the finger data which includes the finger's ID, X and Y coordinates, the Z magnitude and on-chip gestures detected. When a finger is detected on the screen, it is assigned an ID, and while that finger remains in contact with the screen the Finger ID remains the same. In this way a host can uniquely identify and easily track the fingers. There is a status bit that indicates if a touch or set of touches matches the signature of a large object, as well as a count of the number of touches in case more than one finger is on the screen.

Table 4 on page 10 defines the Operating mode register map for the CY8CTST242.

System Information mode allows access to and control over the information not used on a regular basis, for instance device or revision IDs and set the parameters that control the power states. System Information mode also allows access to the built-in manufacturing test functionality. The three registers that control the power states, Active Refresh Interval, Touch Timeout and Low Power Refresh Interval, are accessed in system information mode. For more information on these registers, refer to the "Power States Summary" on page 5. Table 5 on page 11 defines the System Information mode register map for the CY8CTST242.

Test mode allows for characterization of the panel. This mode enables a large amount of data to be read, but without the requirement of the fastest possible refresh rate. This device mode is often used as part of automated tests. When in Test mode, the active distance is automatically set to zero and the power states are disabled, enabling continuous communication. The following data are available in test mode:

- Raw data for all sensors
- Signal data for all sensors
- Calibration data for all sensors

Table 6 on page 12 defines the Test mode register map for the CY8CTST242

Operating Mode Register Map

For more information on Operating mode, the CY8CTST242 protocols in general and the details of all registers, refer to the *TrueTouch™ Standard Products Platform Technical Reference Manual (TRM)*.

Table 4. CY8CTST242 Operating Mode Register Map

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Host Access
00h	HST_MODE	Data Read Toggle	Device Mode[2:0]				Low Power	Deep Sleep	Soft Reset	RW
01h	TT_MODE	New Data Counter[1:0]		Buffer Invalid	Bootloader Flag					R
02h	TT_ STAT			Object Detect[2:0]		Number of Touches[3:0]				R
03h	TOUCH1_XH	1st Touch X Position[15:8]								R
04h	TOUCH1_XL	1st Touch X Position[7:0]								R
05h	TOUCH1_YH	1st Touch Y Position[15:8]								R
06h	TOUCH1_YL	1st Touch Y Position[7:0]								R
07h	TOUCH1_Z	1st Touch Z Value[7:0]								R
08h	EVNT_IDX							Event Index [1:0]		R
09h	TOUCH2_XH	2nd Touch X Position[15:8]								R
0Ah	TOUCH2_XL	2nd Touch X Position[7:0]								R
0Bh	TOUCH2_YH	2nd Touch Y Position[15:8]								R
0Ch	TOUCH2_YL	2nd Touch Y Position[7:0]								R
0Dh	Undefined									
0Eh	GEST_CNT	Overflow Flag	Gesture Count[6:0]							R
0Fh	GEST_ID	Gesture ID[7:0]								R
10h	Undefined									
11h	Undefined									
12h	Undefined									
13h	Undefined									
14h	Undefined									
15h	Undefined									
16h	Undefined									
17h	Undefined									
18h	Undefined									
19h	Undefined									
1Ah	Undefined									
1Bh	Undefined									
1Ch	Undefined									
1Dh	Undefined									
1Eh	GEST_SET	Gesture Group 4 Enable	Gesture Group 3 Enable	Gesture Group 2 Enable	Gesture Group 1 Enable	Active Distance[3:0]				W
1Fh	Reserved	Reserved (do not use)								R

R Host read register or bits, host must not write this register.
W Host write register or bits, host can also read this register.
RW Both host and device write register or bits.
Note "Undefined" registers are available for customer-defined extensions.

System Information Mode Register Map

For more information on System Information mode, the CY8CTST242 protocols in general and the details of all registers, refer to the *TrueTouch™ Standard Products Platform Technical Reference Manual (TRM).*

Table 5. CY8CTST242 System Information Mode Register Map

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Host Access
00h	HST_MODE	Data Read Toggle	Device Mode[2:0]				Low Power	Deep Sleep	Soft Reset	RW
01h	MFG_STAT	Pass	Invalid command	Buffer Invalid			Scan Active	Command Complete	Busy	R
02h	MFG_CMD	Manufacturing Test Command [7:0]								W
03h	CID_0	Custom ID #0[7:0]								R
04h	CID_1	Custom ID #1[7:0]								R
05h	CID_2	Custom ID #2[7:0]								R
06h	Undefined									
07h	UID_0*	Unique ID #0[7:0]								R
08h	UID_1*	Unique ID #1[7:0]								R
09h	UID_2	Unique ID #2[7:0]								R
0Ah	UID_3	Unique ID #3[7:0]								R
0Bh	UID_4	Unique ID #4[7:0]								R
0Ch	UID_5	Unique ID #5[7:0]								R
0Dh	UID_6	Unique ID #6[7:0]								R
0Eh	UID_7	Unique ID #7[7:0]								R
0Fh	BL_VERH	Bootloader Version[15:8]								R
10h	BL_VERL	Bootloader Version[7:0]								R
11h	TTS_VERH	TrueTouch Standard Products Version[15:8]								R
12h	TTS_VERL	TrueTouch Standard Products Version [7:0]								R
13h	APP_IDH	Application ID[15:8]								R
14h	APP_IDL	Application ID[7:0]								R
15h	APP_VERH	Application Version[15:8]								R
16h	APP_VERL	Application Version[7:0]								R
17h	Undefined									
18h	Undefined									
19h	Undefined									
1Ah	Undefined									
1Bh	Undefined									
1Ch	Undefined									
1Dh	ACT_INTRVL	Active Refresh Interval[7:0]								W
1Eh	TCH_TMOUT	Touch Timeout[7:0]								W
1Fh	LP_INTRVL	Low Power Refresh Interval7:0]								W

R Host read register or bits, host must not write this register.
W Host write register or bits, host can also read this register.
RW Both host and device write register or bits.* UID_0 and UID_1 contains the values shown as "Unique ID" in Table 25 on page 30.
Note "Undefined" registers are available for customer-defined extensions.

Test Mode Register Map

For more information on Test mode, the CY8CTST242 protocols in general and the details of all registers, refer to the *TrueTouch™ Standard Products Platform Technical Reference Manual (TRM)*.

Table 6. CY8CTST242 Test Mode Register Map

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Host Access
00h	HST_MODE	Data Read Toggle	Device Mode[2:0]				Low Power	Deep Sleep	Soft Reset	RW
01h	TT_MODE	New Data Counter[1:0]		Buffer Invalid	Bootloader Flag					R
02h	TT_STAT			Object Detected [2:0]		Number of Touches[3:0]				R
03h	TOUCH1_XH	1st Touch X Position[15:8]								R
04h	TOUCH1_XL	1st Touch X Position[7:0]								R
05h	TOUCH1_YH	1st Touch Y Position[15:8]								R
06h	TOUCH1_YL	1st Touch Y Position[7:0]								R
07h	SNS_C_0H	Sensor Col 0 Data[15:8]								R
08h	SNS_C_0L	Sensor Col 0 Data[7:0]								R
09h	SNS_C_1H	Sensor Col 1 Data[15:8]								R
0Ah	SNS_C_1L	Sensor Col 1 Data[7:0]								R
. . .	. . .	. . .								. . .
2r + 2c + 05h	SNS_R_(r – 1)H	Sensor Row (r – 1)[15:8]								R
2r + 2c + 06h	SNS_R_(r – 1)L	Sensor Row (r – 1)[7:0]								R

R Host read register or bits, host should not write this register.
W Host write register or bits, host can also read this register.
RW Both host and device write register or bits.
r Number of Y sensors (rows).
c Number of X sensors (columns).

Host Development Kit (HDK)

Cypress supports rapid customer evaluation and host software development with its host development kit (HDK). Using the HDK, a designer can become familiar with the host protocols and the CY8CTST242 touchscreen controllers behavior in all of its modes. The TrueTouch Host Emulator PC GUI acts like the host, and this same program can be configured to work with a customer's panel (using the TrueTouch Bridge) to allow early prototype development, before the final system host is available. Included in this kit is:

- A Cypress evaluation board with a development version of the CY8CTST242 touchscreen controller connected to an ITO touchscreen panel.
- TrueTouch Bridge communications interface between the evaluation board/touchscreen controller and a PC through a provided USB cable. The TrueTouch Bridge provides programming and configuration capability to program different configurations of the CY8CTST242 touchscreen controller and evaluate its features.
- TrueTouch Host Emulator PC software that communicates with the evaluation board (through the TrueTouch bridge) using the communications modes described in section Communications Protocol Summary on page 9.
- Programming files for the evaluation board.
- PSoC Programmer PC software, a standalone tool for programming the CY8CTST242 devices as well as other Cypress programmable devices. PSoC Programmer software is compatible with other Cypress programming hardware including the PSoC MiniProg. PSoC programmer is also available of at http://www.cypress.com/psocprogrammer.

For more information about the HDK supporting the CY8CTST242 touchscreen controller contact your local Cypress sales representative. You can also direct your requests to tsbusdev@cypress.com.

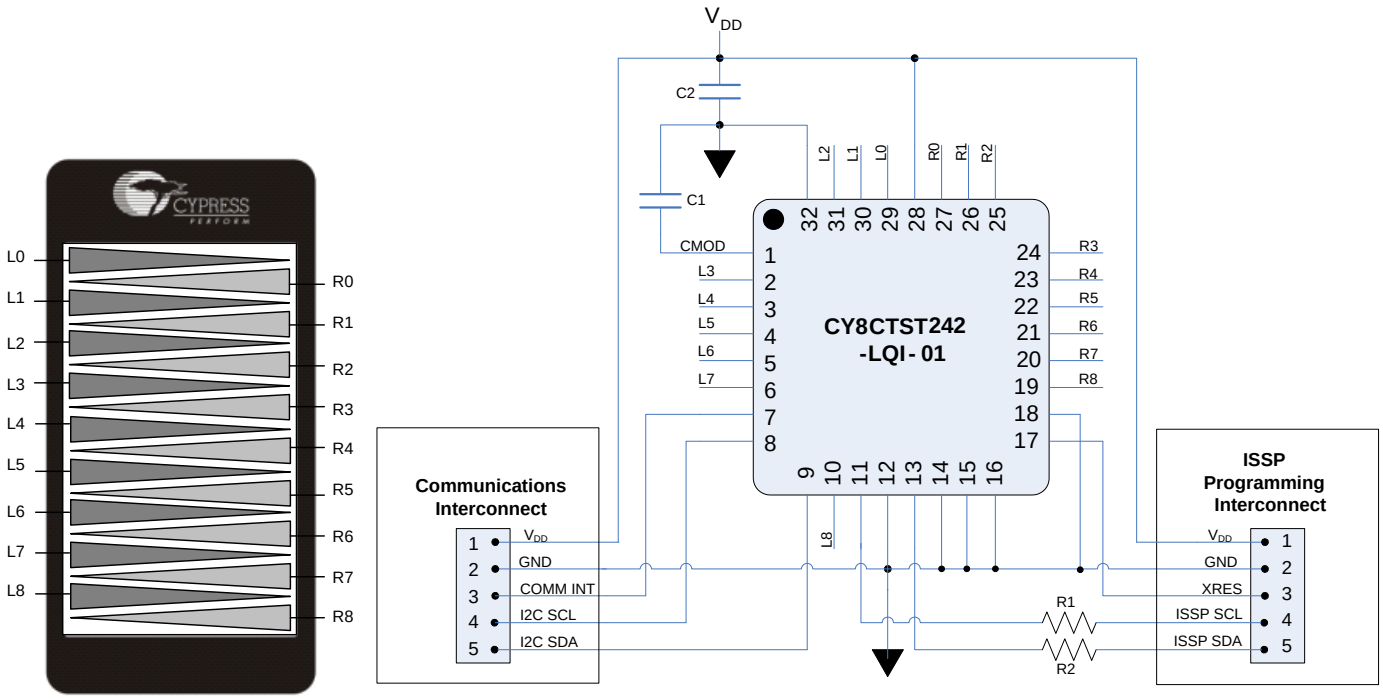
Mobile Device Operating System Driver Support

Cypress TrueTouch devices operate with industry standard and custom host device drivers. Cypress provides drivers for the CY8CTST242 for Android operating systems. Additionally, the Cypress Android driver, because it is provided as open source, can also be repurposed for custom or Linux based operating systems. These Cypress drivers map directly to the Operating and System information modes of the CY8CTST242 touchscreen controller to provide easy integration into any device based on these operating systems. Finally, because the CY8CTST242 device architecture is developed with a standard protocol interface, device drivers can be repurposed for any of the devices in the CY8CTST242 family.

For more information about the drivers supporting the CY8CTST242 touchscreen controller contact your local Cypress sales representative. You can also direct your requests to tsbusdev@cypress.com.

Example Application Schematic

Figure 3. CY8CTST242-LQI-01 Schematic with I²C and ISSP



Component Recommendations

V_{DD}: 1.71 to 5.5V

C1: 0.01 µF, X7R 0402, Ceramic, 6.3 V

C2: 0.1 µF, X7R 0402, Ceramic, 6.3 V

R1: 100 Ω, 1/16W 0402

R2: 100 Ω, 1/16W 0402

Notes

1. Any Ln/Rn net may be connected to any row or column on the ITO sensor. This allows for maximum FPC routing flexibility.

   The "L" and "R" ITO lines are defined by the screen orientation, as shown in graphic to the left. "L" refers to the left side sensors and "R" refers to the right side sensors.

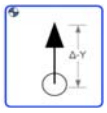
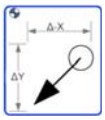
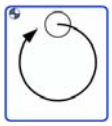
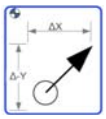
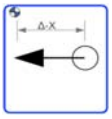
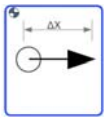
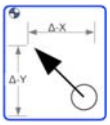
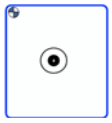
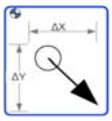
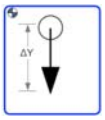
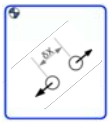
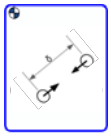
   With this orientation, gesture directions are reported as shown by the compass rose below the handset graphic.

   See *Cypress TrueTouch™ Module Design Best Practices* for information on sensor and FPC routing.
2. Ground unused sensor pins.
3. Use of the Communications Interrupt (COMM INT pin) is optional but strongly recommended. If the Communications Interrupt is not used, pin 7 may be used for an additional ITO sensor pin.
4. In FPC layout, place capacitors as near as possible to package pins. Also, in FPC layout, route INT, SCL, and SDA lines perpendicular to sensor traces or isolate them from sensor traces with GND.
5. Connect the center pad of the CY8CTST242 device to GND.
6. The ISSP Programming Interconnect is optional. It is required if unprogrammed CY8CTST242 devices will be programmed after module assembly. Pins 11 and 13 may be used as additional ITO sensor pins.

Gestures

CY8CTST242 provides support for on-chip gesture determination. Table 7 shows the set of provided gestures. The CY8CTST242 supports gesture detection using one finger. For more information on the provided gestures shown in the table, refer to the TrueTouch Standard Products Platform Technical Reference Manual (TRM).

Table 7. CY8CTST242 Gestures

Gesture ID: Name	Gesture ID: Name	Gesture ID: Name	Gesture ID: Name	Gesture ID: Name	Gesture ID: Name
0x10: Single Touch Pan North		0x1A: Single Touch Pan Southwest		0x28: Single Touch Rotate Clockwise	
0x12: Single Touch Pan Northeast		0x1C: Single Touch Pan West		0x29: Single Touch Rotate Counter Clockwise	
0x14: Single Touch Pan East		0x1E: Single Touch Pan Northwest		0x2F: Touch Down	
0x16: Single Touch Pan Southeast		0x20: Single Touch Single Click		0x4F: Lift Off	
0x18: Single Touch Pan South		0x22: Single Touch Double Click		0x48: Zoom in[21]	
0x49: Zoom out[21]					

Note
21. A minimum of at least electrode spacing is required for two-finger gestures.

Touchscreen System Specifications

This section specifies the touchscreen system performance delivered by the CY8CTST242 controller.

Table 8 lists the typical performance delivered by the CY8CTST242 touchscreen controller with a true single layer ITO touchscreen sensor.

Table 8. Single Layer Sensor Performance Specifications

Parameter	Description	Conditions	Typ	Units
ACC_{CORE}	Typical accuracy error excluding edge	Excludes a 4.5 mm border; applies to a 9 mm finger	1.25	mm
ACC_{FULL}	Typical accuracy error across full panel	Entire panel, applies to finger 9 mm	2.0	mm
LIN_{CORE}	Typical linearity error excluding edge	Excludes a 4.5 mm border; applies to a 9 mm finger; finger moving at 50 mm/s	0.75	mm
LIN_{FULL}	Typical linearity error across whole panel	Entire panel, applies to 9 mm; finger moving at 50 mm/s	1.0	mm
NFR	Noise free resolution	Customer-defined resolution does not limit maximum resolution	0.2	mm
TREFRESH	Maximum refresh time of touchscreen panel data in active state	One finger present on panel, active interval (ACT_INTRVL) set to 0	8.6	ms
$TRESP_{ACT}$	Maximum response time to a touch in active state	Active interval (ACT_INTRVL) set to 0, low power disabled, no finger on panel before touch	17.2	ms
$TRESP_{LP}$	Maximum response time to a touch in low power state	Active interval (ACT_INTRVL) set to 16ms, low power refresh interval (LP_INTRVL) set to 50 ms, no finger on panel before touch	70	ms
$TRESP_{DS}$	Maximum time to transition to active state from deep sleep state		100	ms
IDD_{AVG}	Active state average digital supply current	Active interval (ACT_INTRVL) set to 16, one finger on panel	2	mA
IDD_{LP}	Low power state average digital supply current	Low power refresh interval (LP_INTRVL) set to 50 ms, no finger on panel	0.7	mA
IDD_{DS}	Deep sleep state average supply current	Wake from deep sleep state only from COMM INT pin edge	100	nA

Performance Conditions

Table 9 lists the required conditions for the True Single Layer Sensor ITO panel/touchscreen module that must be met in order to guarantee the system performance specifications delivered by the CY8CTST242 touchscreen controller. Cypress works with many qualified touchscreen and ITO sensor providers to design the touchscreen to these specifications.

Table 9. Single Layer Sensor Performance Conditions

Parameter	Description	Notes	Min	Max	Units
V_{DD}	Digital supply voltage input range	Voltage ripple ≤ 70 mV	1.71	5.5	V
T_{OP}	Operating temperature range		–20	70	°C
T_{ROC}	Temperature rate of change		–10	10	°C/min
HUM	Relative humidity		0	95	%
DFG	Size of finger, diameter		6	10	mm
DSS_{LCS}	Size of the screen	Measured diagonally	–	3.5	inches
DSP_{LCS}	Sensor pitch		–	9.5	mm
DLG_{LCS}	LCD air gap		0.2	–	mm
DCT_{LCS_GLASS}	Glass cover thickness	No shield required	0.7	1.2	mm
DCT_{LCS_PMMA}	PMMA cover thickness	To prevent panel flexing, a shield layer is required if PMMA cover lens is used with PET substrate.	0.5	1	mm
KCD	Cover dielectric		3	8	
Note Requires use of a Cypress-qualified ITO partner; Cypress Sales can help you determine if your vendor is qualified.					

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CTST242 TrueTouch devices.

Absolute Maximum Ratings

Table 10. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage temperature	Higher storage temperatures reduces data retention time. Recommended Storage Temperature is +25°C ± 25°C. Extended duration storage temperatures above 85°C degrades reliability.	–55	+25	+125	°C
V_{DD}	Supply voltage relative to Vss		–0.5	–	+6.0	V
V_{IO}	DC input voltage		Vss –0.5	–	V_{DD} + 0.5	V
V_{IOZ}	DC voltage applied to tristate		Vss –0.5	–	V_{DD} + 0.5	V
I_{MIO}	Maximum current into any port pin		–25	–	+50	mA
ESD	Electrostatic discharge voltage	Human body model ESD.	2000	–	–	V
LU	Latch up current	In accordance with JESD78 standard.	–	–	200	mA

Device Operating Temperature

Table 11. Device Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient temperature		–40	–	+85	°C
T_C	Commercial temperature range		0	–	70	°C
T_J	Operational die temperature	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 29. The user must limit the power consumption to comply with this requirement.	–40	–	+100	°C

DC Chip Level Specifications

Table 12 lists guaranteed maximum and minimum specifications for –40 °C ≤ T_A ≤ 85 °C. Typical values are measured at T_A = 25 °C.

Table 12. DC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD}[22, 23]	Digital supply voltage input range		1.71	2.8	5.5	V
V_{POR}	Voltage level below which the device performs a power-on-reset (POR)	V_{DD} must be greater than or equal to 1.71V during startup, reset from the XRES pin, or reset from watchdog	1.61	1.66	1.71	V

Notes

22. When V_{DD} remains in the range from 1.71 V to 1.9 V for more than 50 µsec, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 usec to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SRPOWER_UP parameter (see Table 18).
23. If the drop in V_{DD} exceeds 5% of the base V_{DD}, the rate at which V_{DD} drops should not exceed 200 mV/s. Base V_{DD} can be between 1.8 V and 5.5 V.

DC General Purpose I/O Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C TA ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ TA ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ TA ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 13. 3.3 V to 5 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull up resistor		4	5.6	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 Pins	$I_{OH} \leq 10$ µA, maximum of 10 mA source current in all I/Os.	V_{DD} – 0.2	–	–	V
V_{OH2}	High output voltage Port 2 or 3 Pins	I_{OH} = 1 mA, maximum of 20 mA source current in all I/Os.	V_{DD} – 0.9	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator disabled for port 1	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os.	V_{DD} – 0.2	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator disabled for port 1	I_{OH} = 5 mA, maximum of 20 mA source current in all I/Os.	V_{DD} – 0.9	–	–	V
V_{OH5}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	I_{OH} < 10 µA, V_{DD} > 3.1 V, maximum of 4 I/Os all sourcing 5 mA.	2.85	3.00	3.3	V
V_{OH6}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	I_{OH} = 5 mA, V_{DD} > 3.1 V, maximum of 20 mA source current in all I/Os.	2.20	–	–	V
V_{OH7}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I_{OH} < 10 µA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os.	2.35	2.50	2.75	V
V_{OH8}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I_{OH} = 2 mA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os.	1.90	–	–	V
V_{OH9}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} < 10 µA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os.	1.60	1.80	2.1	V
V_{OH10}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os.	1.20	–	–	V
V_{OL}	Low output voltage	I_{OL} = 25 mA, V_{DD} > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).	–	–	0.75	V
V_{IL}	Input low voltage		–	–	0.80	V
V_{IH}	Input high voltage		2.00	–		V
V_H	Input hysteresis voltage		–	80	–	mV
I_{IL}	Input leakage (absolute value)		–	1	1000	nA
C_{PIN}	Pin capacitance	Package and pin dependent. Temp = 25 °C.	0.5	1.7	5	pF

Table 14. 2.4 V to 3.0 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull up resistor		4	5.6	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 pins	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os.	V_{DD} – 0.2	–	–	V
V_{OH2}	High output voltage Port 2 or 3 pins	I_{OH} = 0.2 mA, maximum of 10 mA source current in all I/Os.	V_{DD} – 0.4	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator disabled for port 1	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os.	V_{DD} – 0.2	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator disabled for port 1	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os.	V_{DD} – 0.5	–	–	V
V_{OH5A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} < 10 µA, V_{DD} > 2.4 V, maximum of 20 mA source current in all I/Os.	1.50	1.80	2.1	V
V_{OH6A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, V_{DD} > 2.4V, maximum of 20 mA source current in all I/Os.	1.20	–	–	V
V_{OL}	Low output voltage	I_{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]).	–	–	0.75	V
V_{IL}	Input low voltage		–	–	0.72	V
V_{IH}	Input high voltage		1.4	–		V
V_H	Input hysteresis voltage		–	80	–	mV
I_{IL}	Input leakage (absolute value)			1	1000	nA
C_{PIN}	Pin capacitance	Package and pin dependent. Temp = 25 °C.	0.5	1.7	5	pF

Table 15. 1.71 to 3.3 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull up resistor		4	5.6	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 pins	I_{OH} = 10 µA, maximum of 10 mA source current in all I/Os.	V_{DD} – 0.2	–	–	V
V_{OH2}	High output voltage Port 2 or 3 pins	I_{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os.	V_{DD} – 0.5	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator disabled for port 1	I_{OH} = 100 µA, maximum of 10 mA source current in all I/Os.	V_{DD} – 0.2	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator disabled for port 1	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os.	V_{DD} – 0.5	–	–	V
V_{OL}	Low output voltage	I_{OL} = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]).	–	–	0.4	V
V_{IL}	Input low voltage		–	–	0.3 × V_{DD}	V

Table 15. 1.71 to 3.3 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input high voltage		0.65 × V_{DD}	–		V
V_H	Input hysteresis voltage		–	80	–	mV
I_{IL}	Input leakage (absolute value)		–	1	1000	nA
C_{PIN}	Pin capacitance	Package and pin dependent. Temp = 25°C.	0.5	1.7	5	pF

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. DC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{SW}	Switch resistance to common analog bus		–	–	800	Ω
R_{GND}	Resistance of initialization switch to Vss		–	–	800	Ω

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8 V.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 17. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{DDIWRITE}$	Supply voltage for flash write operations		1.71	–	5.25	V
I_{DDP}	Supply current during programming or verify		–	5	25	mA
V_{ILP}	Input low voltage during programming or verify	See appropriate DC General Purpose I/O Specifications table.	–	–	V_{IL}	V
V_{IHP}	Input high voltage during programming or verify	See appropriate DC General Purpose I/O Specifications table.	V_{IH}	–	–	V
I_{ILP}	Input current when applying Vilp to P1[0] or P1[1] during programming or verify	Driving internal pull down resistor.	–	–	0.2	mA
I_{IHP}	Input current when applying Vihp to P1[0] or P1[1] during programming or verify	Driving internal pull down resistor.	–	–	1.5	mA
V_{OLP}	Output low voltage during programming or verify		–	–	Vss + 0.75	V
V_{OHP}	Output high voltage during programming or verify	See appropriate DC General Purpose I/O Specifications table. For V_{DD} > 3V use V_{OH4} in Table on page 19.	V_{OH}	–	Vdd	V
$Flash_{ENPB}$	Flash write endurance	Erase/write cycles per block.	50,000	–	–	Cycles
$Flash_{DR}$	Flash data retention	Following maximum flash write cycles, ambient temperature of 55 °C	20	–	–	Years

AC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{XRST}	External reset pulse width		1	–	–	ms
t_{XRST2}	External reset pulse width after power-up[24]	Applies after part has booted	10	–	–	µs
SR_{POWER_UP}	Power supply slew rate	V_{DD} slew rate during power up	–	–	250	V/ms

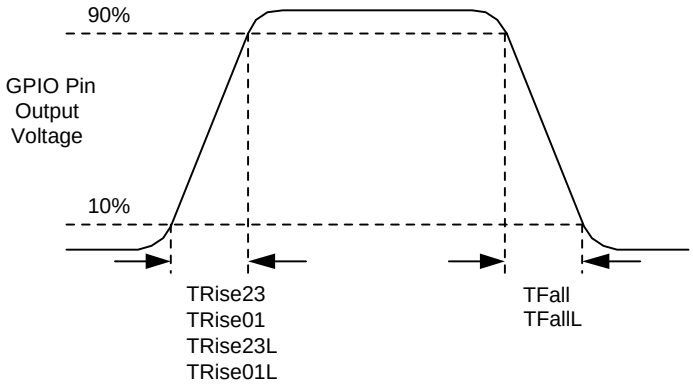
AC GPIO Output Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. AC GPIO Output Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode, Port 1.	0	–	6 MHz for 1.71 V < V_{DD}< 2.4 V 12 MHz for 2.4 V < V_{DD} <5.5 V	MHz
T_{RISE23}	Rise time, strong mode, Cload = 50 pF Ports 2 or 3	V_{DD} = 3.0 to 3.6V, 10% – 90%	15	–	80	ns
$T_{RISE23L}$	Rise time, strong mode low supply, Cload = 50 pF Ports 2 or 3	V_{DD} = 1.71 to 3.0V, 10% – 90%	15	–	80	ns
T_{RISE01}	Rise time, strong mode, Cload = 50 pF Ports 0 or 1	V_{DD} = 3.0 to 3.6V, 10% – 90%. LDO enabled or disabled.	10	–	50	ns
$T_{RISE01L}$	Rise time, strong mode low supply, Cload = 50 pF Ports 0 or 1	V_{DD} = 1.71 to 3.0V, 10% – 90%. LDO enabled or disabled.	10	–	80	ns
T_{FALL}	Fall time, strong mode, Cload = 50 pF All ports	V_{DD} = 3.0 to 3.6V, 10% – 90%	10	–	50	ns
T_{FALLL}	Fall time, strong mode low supply, Cload = 50 pF All Ports	V_{DD} = 1.71 to 3.0 V, 10% – 90%	10	–	70	ns

Figure 4. GPIO Timing Diagram

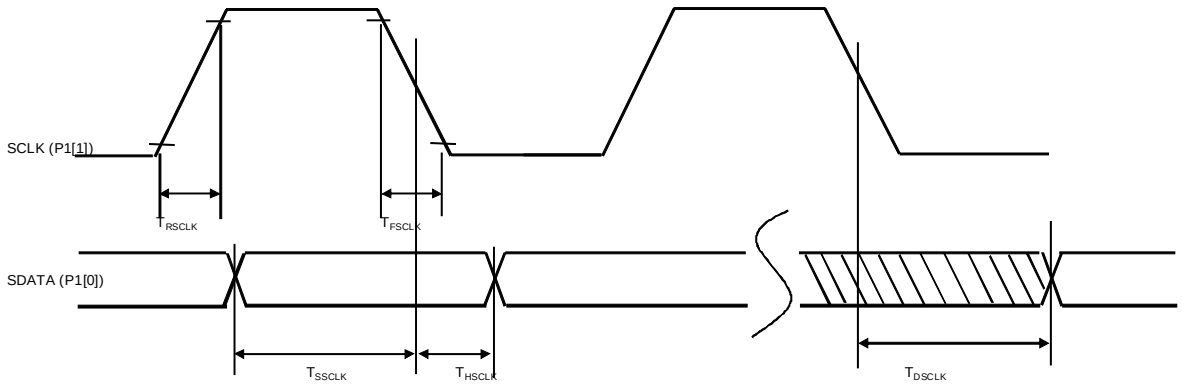


Note

24. The minimum required XRES pulse length is longer when programming the device (see <HyperText>Table 20 on page 23).

AC Programming Specifications

Figure 5. AC Waveform



The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 20. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{RSCLK}	Rise time of SCLK		1	–	20	ns
T_{FSCLK}	Fall time of SCLK		1	–	20	ns
T_{SSCLK}	Data setup time to falling edge of SCLK		40	–	–	ns
T_{HSCLK}	Data hold time from falling edge of SCLK		40	–	–	ns
F_{SCLK}	Frequency of SCLK		0	–	8	MHz
T_{ERASEB}	Flash erase time (Block)		–	–	18	ms
T_{WRITE}	Flash block write time		–	–	25	ms
T_{DSCLK}	Data out delay from falling edge of SCLK	$3.6 < V_{DD}$	–	–	60	ns
T_{DSCLK3}	Data out delay from falling edge of SCLK	$3.0 \le V_{DD} \le 3.6$	–	–	85	ns
T_{DSCLK2}	Data out delay from falling edge of SCLK	$1.71 \le V_{DD} \le 3.0$	–	–	130	ns
T_{XRST3}	External reset pulse width after power up	Required to enter programming mode when coming out of sleep	300	–	–	µs
T_{XRES}	XRES Pulse Length		300	–	–	µs
$T_{VDDWAIT}$	V_{DD} stable to wait-and-poll hold off		0.1	–	1	ms
$T_{VDDXRES}$	V_{DD} stable to XRES assertion delay		14.27	–	–	ms
T_{POLL}	SDATA high pulse time		0.01	–	200	ms
T_{ACQ}	“Key window” time after a V_{DD} ramp acquire event, based on 256 ILO clocks.		3.20	–	19.60	ms
$T_{XRESINI}$	“Key window” time after an XRES event, based on 8 ILO clocks		98	–	615	µs

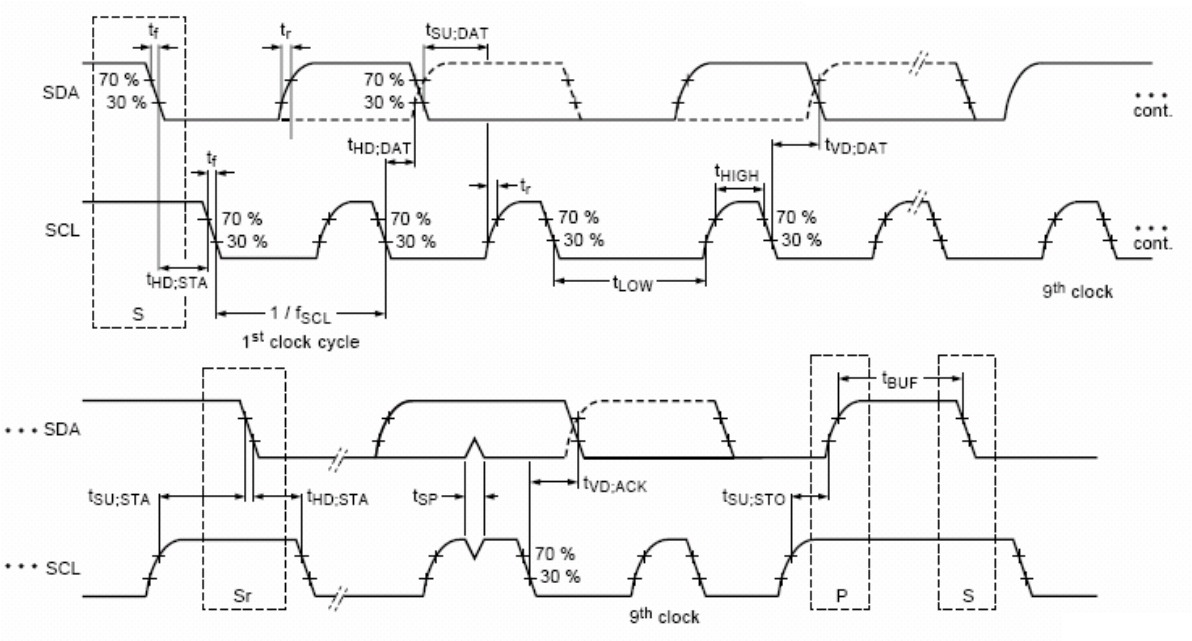
I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 21. AC Characteristics of the I2C SDA and SCL Pins

Symbol	Description	Conditions	Min	Max	Units
F_{SCLI2C}	SCL clock frequency		0	400	kHz
$T_{HDSTAI2C}$	Hold time (repeated) Start condition. After this period, the first clock pulse is generated.		0.60	–	µs
T_{LOWI2C}	LOW period of SCL clock		1.3	–	µs
$T_{HIGHI2C}$	HIGH period of SCL clock		0.60	–	µs
$T_{SUSTAI2C}$	Setup time for repeated Start condition		0.60	–	µs
$T_{HDDATI2C}$	Data hold time		0	–	µs
$T_{SUDATI2C}$	Data setup time		100	–	ns
$T_{SUSTOI2C}$	Setup time for STOP condition		0.60	–	µs
T_{BUFI2C}	Bus free time between a Stop and Start condition		1.3	–	µs
T_{SPI2C}	Pulse width of spikes that are suppressed by input filter	I²C Specification 3.0 maximum is 50 ns	0	50	ns
C_{BUS}	Capacitance load for SDA or SCL		–	200[25]	pF

Figure 6. Timing Diagram for Fast/Standard Mode of the I2C Bus



Legend

S I²C Start Condition

Sr I²C Repeat Start Condition

P I²C Stop Condition

Note

25. This does not fully meet the I2C max capacitive load targets of 400 pF.

SPI Specifications

CY8CTST242 supports all SPI slave modes. The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 22. AC Characteristics of the SPI Pins

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency		–	–	2	MHz
SDR_{SPI}	Sustained data rate for SPI transaction – for SCLK > 2 MHz, host must add break between bytes		–	–	2	Mbps
$T_{IDLESPI}$	Time between consecutive SPI transactions (duration between ~SS deactivation and the following ~SS activation)		8	–	–	µs
T_{LOW}	SCLK low time		42	–	–	ns
T_{HIGH}	SCLK high time		42	–	–	ns
T_{SETUP}	MOSI to SCLK setup time		30	–	–	ns
T_{HOLD}	SCLK to MOSI hold time		50	–	–	ns
T_{SS_MISO}	SS low to MISO valid		–	–	153	ns
T_{SCLK_MISO}	SCLK to MISO valid		–	–	125	ns
T_{SS_HIGH}	SS high time		50	–	–	ns
T_{SS_SCLK}	Time from SS low to first SCLK		200	–	–	ns
T_{SCLK_SS}	Time from last SCLK to SS high		200	–	–	ns

Figure 7. SPI Protocol Timing Diagram

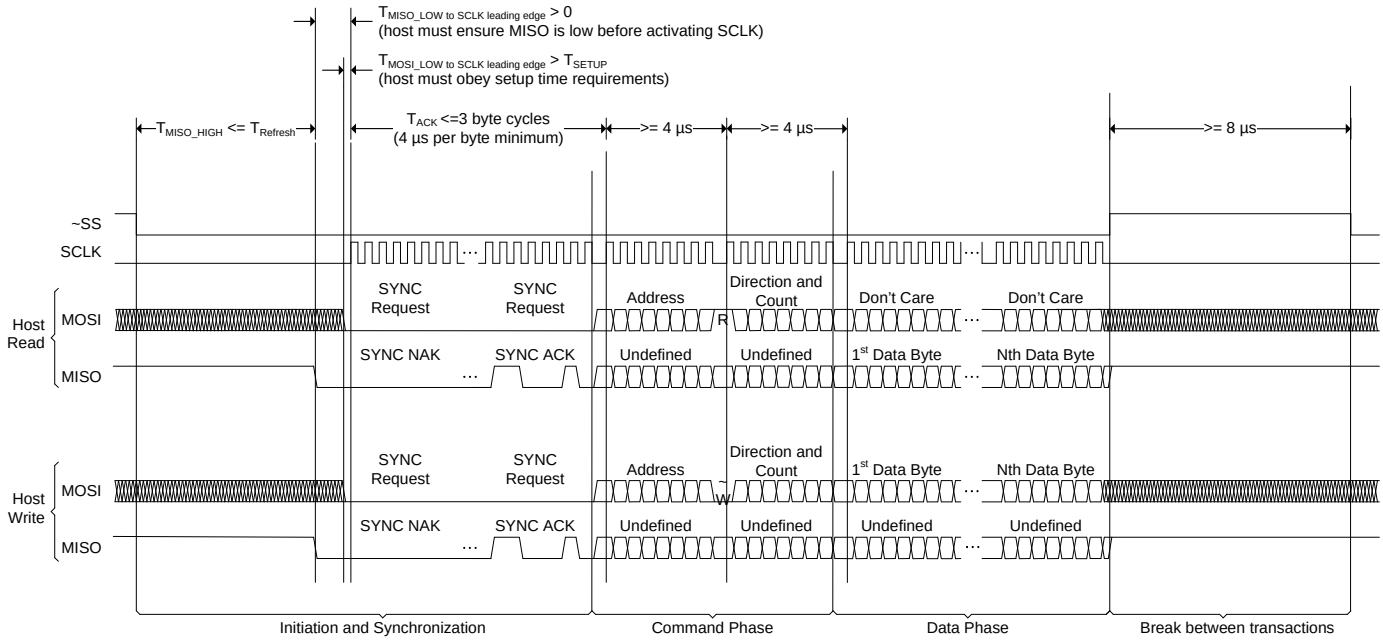


Figure 8. SPI Slave Mode 0 and 2

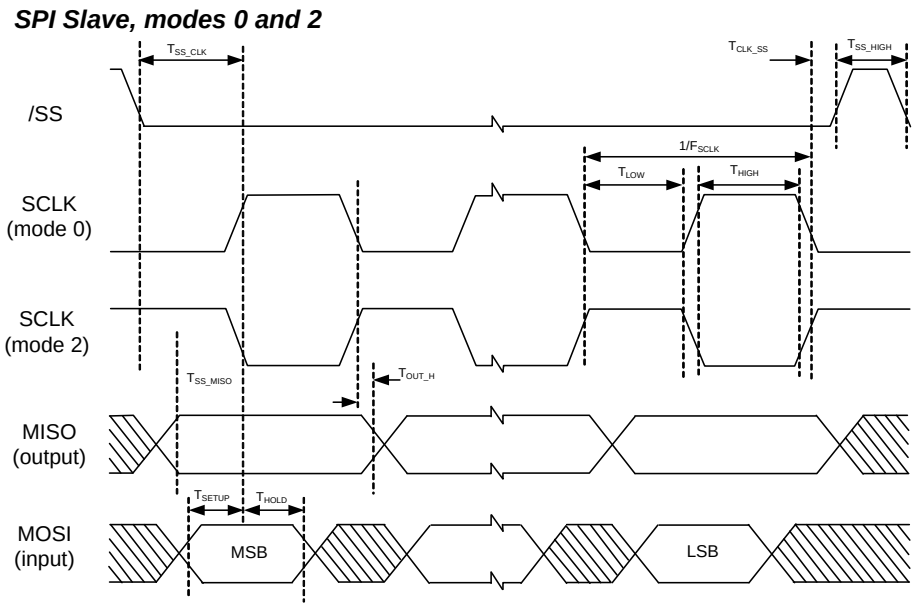
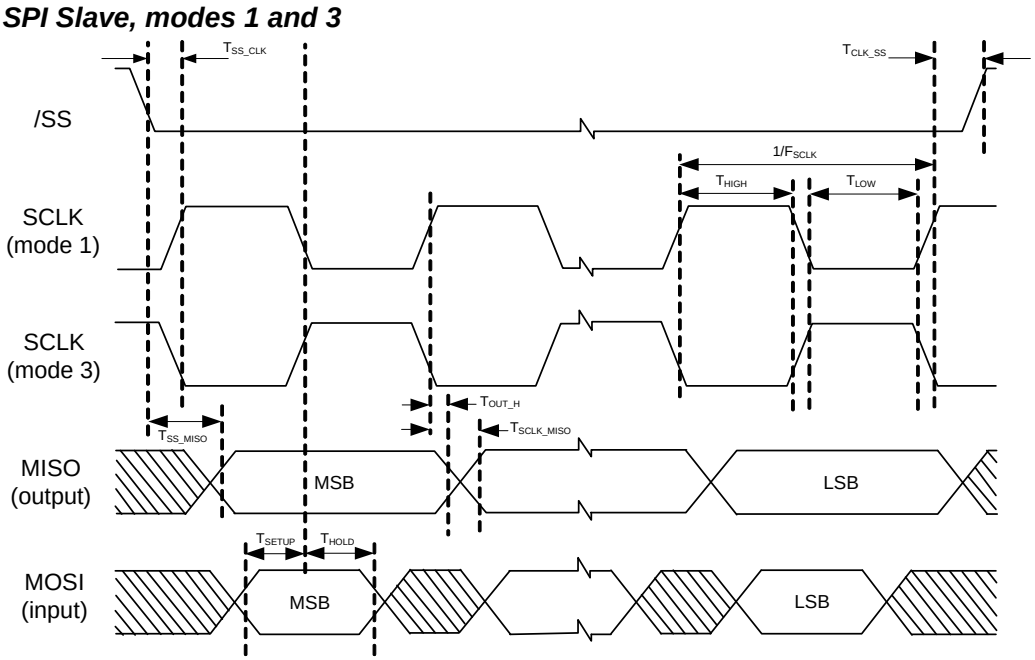


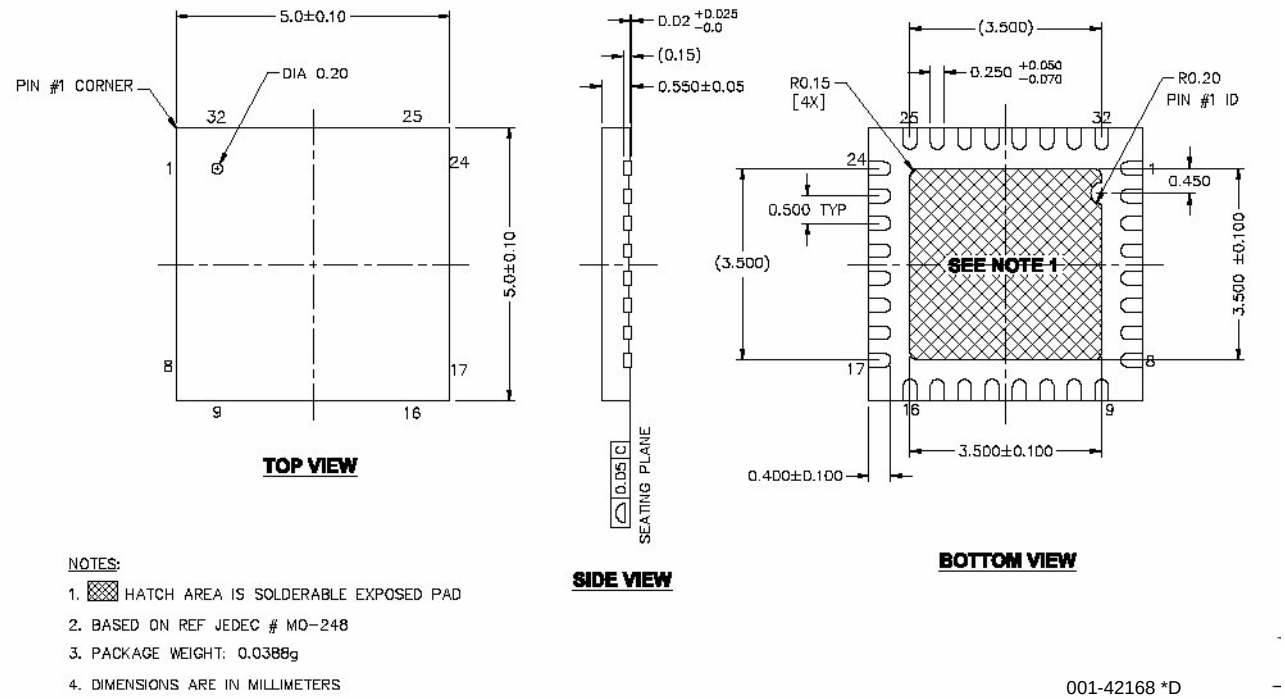
Figure 9. SPI Slave Mode 1 and 3



Packaging Information

This section illustrates the packaging specifications for the CY8CTST242 devices.

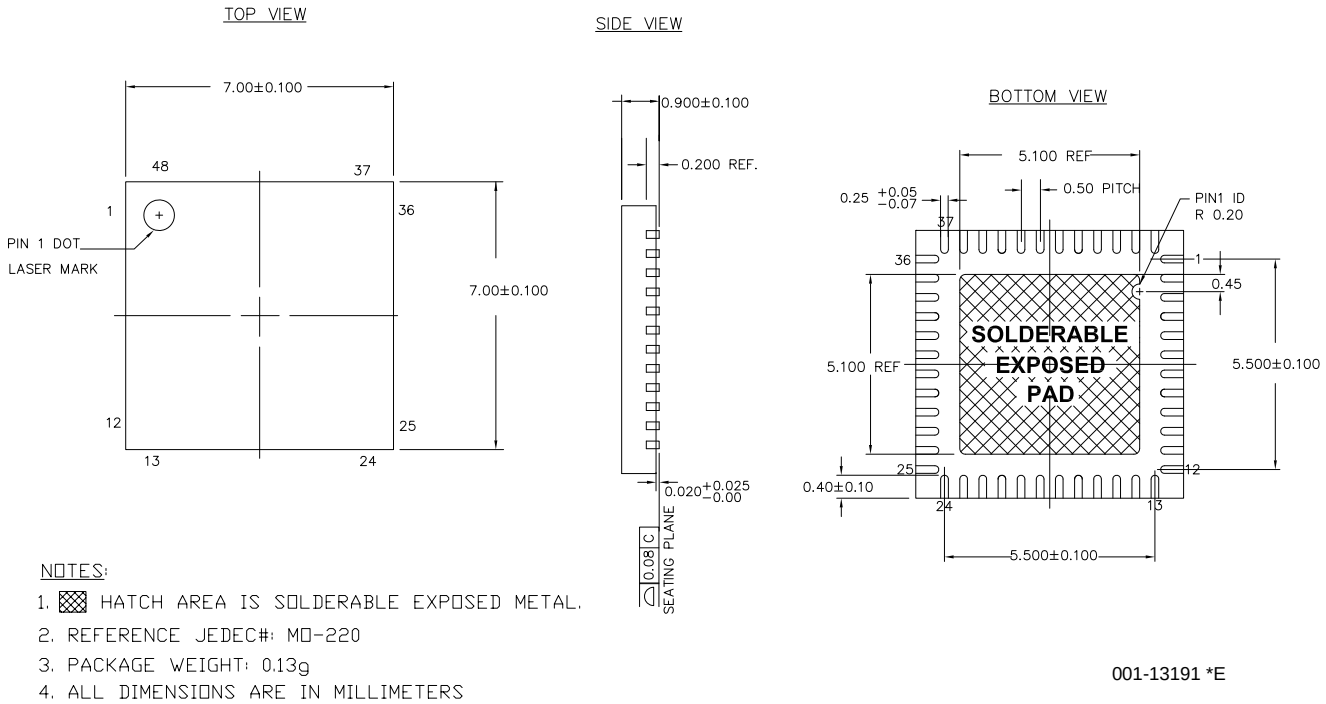
Figure 10. 32-Pin (5 × 5 × 0.55 mm) QFN



Important Note

For information on the preferred dimensions for mounting QFN packages, see the application notes at Application Notes for Surface Mount Assembly of Amkor's *Micro*LeadFrame® (MLF®) Packages.

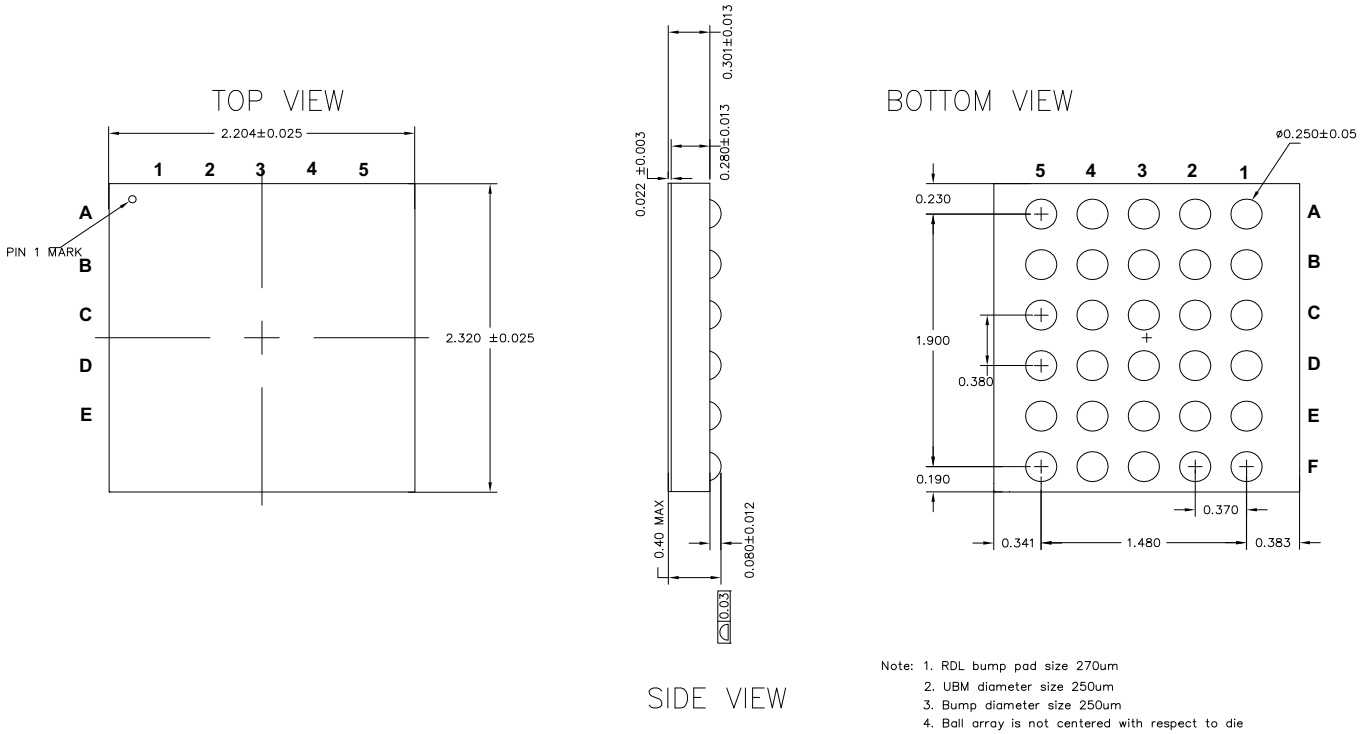
Figure 11. 48-Pin (7 × 7 mm) QFN



Important Note

For information on the preferred dimensions for mounting QFN packages, see the application notes at Application Notes for Surface Mount Assembly of Amkor's *Micro*LeadFrame® (MLF®) Packages.

Figure 12. 30-Ball (2.2 × 2.32 × 0.40 mm) WLCSP



* ALL DIMENSION ARE IN MILLIMETER
Package weight : 0.004g
Jedec Publication 95

001-50669 *B

Important Note

For information on the preferred dimensions for mounting CSP packages, see the application note AN69061: Design Guidelines for Using Cypress Wafer-Level Chip Scale Package (WLCSP).

Thermal Impedances

Table 23. Thermal Impedances per Package

Package	Typical θ_{JA} [26]
32 Pin QFN	20 °C/W
48 Pin QFN[27]	18 °C/W
30 Ball WLCSP	54 °C/W

Solder Reflow Peak Temperature

Table 24 lists the maximum solder reflow peak temperatures. Thermal ramp rate during preheat should be 3 °C/s or lower

Table 24. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
32 Pin QFN	260 °C	30 s
48 Pin QFN	260 °C	30 s
30 Ball WLCSP	260 °C	30 s

Notes
26. $T_J = T_A$ + Power x θ_{JA}.
27. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

Ordering Information

The following table lists the TrueTouch Standard Product Single Touch Touchscreen Controllers. For information on other TrueTouch families, visit http://www.cypress.com/truetouch.

Table 25. Device Ordering Information

Part Number	TrueTouch						Sensor		Minimum Interface Voltage	Supply Voltage Operating Range	Bootloader	I²C	SPI	UART	Package
	Typical Screen Size (in.) (4:3 Aspect Ratio)	Maximum Nodes	Maximum Fingers	On-chip Gesture Decoding	True Single Layer Sensor	Large Object Detection	Glass	Film							
CY8CTST242-LQI-01(T)	3.5	24	2	✔	✔	✔	✔	✔	1.8	1.71-5.5	✔	✔	✔	✔	32 Pin QFN
CY8CTST242-LTI-01(T)	3.5	32	2	✔	✔	✔	✔	✔	1.8	1.71-5.5	✔	✔	✔	✔	48 Pin QFN
CP8CTST242-FNC-01T	3.5	24	2	✔	✔	✔	✔	✔	1.8	1.71-5.5	✔	✔	✔	✔	30 Ball WLCSP

Ordering Code Definitions

Cx8 C TST 242 - xxx xx(T)

Feature Set: (T=Tape and Reel)
01 = Basic feature set

Pins/Package Type:
LQI = 36-Pin 0.6 mm Height QFN, Industrial grade
LTI = 48-Pin 1.0 mm Height QFN, Industrial grade
FNC = 30-Ball 0.4 mm Height WLCSP, Commercial grade

Sub-family Identifier

Family Code: TST = SingleTouch Controller

Technology Code: C = CMOS

Marketing Code: CY8 = Cypress PSoC
CP8 = Custom part Cypress PSoC

Acronyms

Table 26. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
CPU	central processing unit
CSP	chip scale package
EP	exposed pad
ESD	electrostatic discharge
FPC	flexible printed circuit
GPIO	general purpose input/output
GUI	graphical user interface
HDK	host development kit
ILO	internal low speed oscillator
IMO	internal main oscillator
ISSP	in-system serial programming
ITO	indium tin oxide
I^2C	inter-integrated circuit
I/O	input/output
LCD	liquid crystal display
LDO	low dropout regulator
OLED	organic light emitting diode
PCB	printed circuit board
POR	power on reset
PSoC®	Programmable System-on-Chip™
QFN	quad flat no-lead
QVGA	quarter video graphics array
RF	radio frequency
SCL	serial I^2C clock
SCLK	serial ISSP clock
SDA	serial I^2C data
SDATA	serial ISSP data
SNR	signal-to-noise ratio
SPI	serial peripheral interface
SRAM	static random access memory
TRM	technical reference manual
UART	universal asynchronous receiver/transmitter
USB	universal serial bus
XRES	external reset

Document Conventions

Table 27. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
kHz	kilohertz
kΩ	kilohms
Mbps	megabits per second
MHz	megahertz
µA	microamperes
µF	microfarads
µs	microseconds
µV	microvolts
µW	microwatts
mA	milliamperes
min	minute
mm	millimeters
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
Ω	ohms
pF	picofarads
V	volt

Port Nomenclature

Px[y] describes a particular bit ‘y’ available within an I/O port ‘x’. For example, P4[2] reads ‘port 4, bit 2’.

Bit Field Nomenclature

z[x:y] describes a particular range of bits ‘x to y’ within a register named ‘z’. For example, TSNV[15:11] refers to bits 15 through 11 within a register named TSNV.

Reference Documents

Reference documents are available through your local Cypress sales representative. You can also direct your requests to tsbusdev@cypress.com.

- 001-55166 – TrueTouch™ Standard Products Platform Technical Reference Manual (TRM). Contains detailed information on communication protocol, modes and registers, power states, and instructions on getting started with supporting tools.
- 001-49389 – TrueTouch™ Performance Parameters. Contains Cypress touchscreen parameter definitions, justification for parameters, and parameter test methodologies.
- 001-50467 – TrueTouch™ Touchscreen Module Design Best Practices. A system-level design guide for building a capacitive touchscreen module, covering topics such as touchscreen traces, shielding, mechanical design, FPC or PCB design, and LCD considerations.
- 001-56148 – TrueTouch™ Touchscreen Module Integration Best Practices. Describes the best practices to be followed when integrating a touchscreen module into a completed end-product in its final form factor, from completion of touchscreen module bench testing to production readiness.
- 001-57631 – In-System Serial Programming (ISSP) Protocol for CY8C20X36, CY8C20X46, CY8C20X66, CY8C20X96, CY8C20X36A, CY8C20X46A, CY8C20X66A, CY8C20X96A, CY8CTMG2XX, and CY8CTST2XX - AN2026C. Contains information and directions for externally programming a CY8CTXX2XX device.
- 001-59389 – Host Sourced Serial Programming for CY8C20XX6, CY8CTMG2XX, and CY8CTST2XX - AN59389. Contains information and directions for programming a CY8CTXX2XX device from the system host processor.
- AN69061 – Design Guidelines for Using Cypress Wafer-Level Chip Scale Package (WLCSP)
- 001-65973 – CY8C20XX6A/H CapSense® Design Guide

Glossary

ACC_{CORE}	The maximum position error across a pre-defined area of the touchscreen (excluding a one-sensor-wide edge area), as measured in units of distance along a straight line between the actual finger position and the reported finger position.
ACC_{FULL}	The maximum position error across the entire touchscreen, as measured in units of distance along a straight line between the actual finger position and the reported finger position.
active distance	The initial pixel displacement that must be exceeded for a movement to be recognized by the TrueTouch controller.
active time	The sum of scan and process times.
All-Points	Cypress brand name for TrueTouch devices capable of unlimited number of independent finger tracking.
C_F	The change in capacitance when a finger is placed on the touchscreen. C_F is the signal the controller measures.
conversion	The process of measuring the capacitance of a sensor connected to a pin (self capacitance) or capacitance between a pair of sensors connected to different pins (mutual capacitance). The result is a number that can be processed by the CPU. A conversion result is made available to the CPU after digital integration is complete.
D_{FS}	The minimum center-to-center distance between two fingers placed on the touchscreen while two separate fingers are still reported by the touchscreen controller.
LIN_{CORE}	The maximum error from a line drawn across a pre-defined area of the touchscreen (excluding a one-sensor-wide edge area), as measured in units of distance along a perpendicular line between the actual line drawn and the reported line drawn.
LIN_{FULL}	The maximum error from a line drawn across the entire touchscreen, as measured in units of distance along a perpendicular line between the actual line drawn and the reported line drawn.
mutual capacitance	The capacitance between two sense pins. This includes the capacitance formed between the intersection of TX and RX sensors.
noise free resolution	The minimum jitter-free resolvable distance expressed in millimeters. See Cypress's *TrueTouch™ Touchscreen Controller Performance Parameters* (001-49389) for more information.
RC	The time constant of a row or column sensor.
scan	The conversion of all sensor capacitances to digital values.
sense pin	A pin that can be multiplexed to the RX or TX sections of a channel.
signal-to-noise ratio (SNR)	The ratio between a capacitive finger signal and system noise. See Cypress's *Touchscreen Controller Performance Parameters* (001-049389) for more information.
stackup	Layers of materials of different thicknesses in defined order that make up a touchscreen panel.
T_{ACTIVE}	The time it takes to complete one scan and process the new data. $T_{ACTIVE = TSCAN + TPROCESS}$
$T_{PROCESS}$	The time it takes to process the new digital information after a scan and then signal an interrupt to the host.
$T_{REFRESH}$	The time between two consecutive frames of touchscreen data available in a data buffer while a finger is present on the touchscreen. The refresh rate is a sum of T_{SCAN}, $T_{PROCESS}$, and T_{SLEEP}. The fastest refresh rate is achieved when the sleep time is removed. See Cypress's *TrueTouch™ Touchscreen Controller Performance Parameters* (001-49389) for more information.

T_{RESP}	The time between a finger touchdown event on the touchscreen and the touchscreen controller generating an interrupt signal.
T_{SCAN}	The time it takes to convert all intersection capacitances on the touchscreen to digital values, including all analog and digital integration time.
T_{SLEEP}	The time the device is asleep during $T_{REFRESH}$ in order to reduce average power.

Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3296696	CIT	06/29/2011	New data sheet.

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PSoC 1 | PSoC 3 | PSoC 5

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